ArTeCS Group/DACYA-UCM Overview and Emulation-Related Research

David Atienza (DACYA/UCM)

Nicolas Genko (LSI/EPFL)

Outline

- ArTeCS group
- NoC Emulation project
  1. Overview
  2. Current status
  3. Immediate Planning
- MpSoC Emulation project
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  3. Planning
- Asynchronous group collaboration
  1. Group summary
  2. Research interests

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ArTeCS Group / DACYA-UCM

- Group of Architecture and Technology of Computing Systems

  http://atc.dacya.ucm.es/

- Complutense University of Madrid

  (Dept. of Computer Architecture and Systems Engineering)

Group composition & Funding

- Group leader: Prof. Francisco Tirado
- Other key scientists: Román Hermida, Milagros Fernández
- Faculty staff members: 13
- Ph.D. candidates: 16
- Funding coming mainly from:
  - Spanish Government
  - Complutense University
  - European Union
  - USA-Spain cooperation calls

Who we are…

- **High Performance Computing Working Division**

- **People in charge:**
  - Tirado Fernández, Francisco (PhD)

- **Faculty:**
  - Bautista Paloma, Alfredo (PhD)
  - Olcoz Herrero, Katzalin (PhD)
  - Prieto Matías, Manuel (PhD)
  - Piñuel Moreno, Luis (PhD)
  - Fabero Jiménez, Juan Carlos (PhD)

- **PhD Candidates:**
  - García Sánchez, Carlos
  - Pardines Lence, Inmaculada
  - Pino Gordo, Silvia del
  - Chaver Martinez, Daniel Angel
  - Gómez Pérez, José Ignacio
  - Rojas Gómez, Miguel Angel
  - Tenllado Van Der Reijden, Christian
  - Velasco Cabo, Jose Manuel

- **System Synthesis Working Division**

- **People in charge:**
  - Hermida Correa, Román (PhD)
    Fernández Centeno, Milagros (PhD)

- **Faculty:**
  - Hidalgo Pérez, Ignacio (PhD)
  - Lanchares Dávila, Juan (PhD)
  - Mendías Cuadros, Jose M. (PhD)
  - Garnica Alcazar, Antonio Oscar (PhD)
  - Sánchez-Elez Martin, Marcos (PhD)

- **PhD Candidates:**
  - Atienza Alonso, David
  - Molina Prego, Mª Carmen
  - Miñana, Guadalupe
  - López Alarcón, Sonia
  - Rivera Vélez, Fredy Alexander
  - Peón Quiros, Miguel
  - Pérez Ramas, Javier Basilio

ArTeCS

Dissemination activities

- News bulletin from ArTeCS(half-yearly)

ArTeCSnews

volume I, issue 1
summer 2004

contents:

Presentation

The research activity of the Group of Architecture and Technology of Computing Systems (ArTeCS) of the Complutense University of Madrid is focused on the conception and construction of digital information processing systems, and its efficient application regarding performance, energy consumption, and cost. Within this broad area, the group pays special attention to high-performance processors, distributed computing, embedded systems, and systems-on-chip.

The first steps of the group can be traced back to the 70s, within the "Departamento de Informática y Automática" (Department of Computer Science and Systems Engineering). To this early period belongs IEA-FI, a 16-bit minicomputer that was entirely designed and built at the Department. The group worked for fifteen years in several topics covering different aspects of the computer architecture field (microprogramming and emulation, direct execution of high-level languages, data base architectures, and fault-tolerant architectures). These works inspired the Ph.D. thesis of the older group members.

Around 1980, the group enrolled in a large project with both research and industry aspects. The main goal of that project was the design and implementation of a power station simulator oriented to the training of human operators in both normal and emergency operation procedures. Having several hundreds of input/output signals, and a very large number of state variables, the development of the simulator consumed four years of activity. Several industrial prototypes derived from this project, addressing not only the field of power stations, but the field of automatic train driving.

The power station simulator DIYAC (1984)

By mid-80s the focus of the group moved to the, in those days, emerging area of high-level synthesis of digital systems, from which derives all the research activity that the group has been doing within the generic field of design automation. In addition to high-level synthesis, our group has been working on hardware-software codesign, reconfigurable computing, formal methods for synthesis, asynchronous systems, and other related topics.

The beginning of 90s witnessed a corner point in the evolution of the group due to the creation of the "Facultad de Informática" (Computer Science School). This allowed an outstanding growth of the number of group members, giving pace to the opening of a second main research line devoted to high performance computing.

Along the last 20 years, under the leadership of Prof. Francisco Tirado, the ArTeCS group has followed a set of interacting research lines, which made it possible the consolidation of a team currently composed of 12 faculty members and more than 15 Ph. D. candidates. Funding of the group comes mainly from the Complutense University, the Spanish Government, and the European Union. Furthermore, the group tries to promote international cooperation with leading institutions all over the world, and currently has links, to cooperate in specific projects, with the University of California at Irvine, IMEC (Leuven), the University of Rochester, and the University of Bologna, among others.

Having full awareness of the past, our collective hope is to keep improving our scientific capabilities, contribute to the education of well-skilled computer professionals, and produce innovative research in our field.

As a matter of commitment with accountability and transparency, ArTeCS group has decided to publish a news bulletin each semester. So this issue is the first in a series that will try to summarize our trajectory, goals, and activities. Even knowing the overhead that this publication will mean for us, we hope to appear on time, at each new issue, with relevant information.

The IEA-FI minicomputer: CPU (1973)

FIDIAS: a high-level synthesis tool (1992)

A news bulletin of the
Architecture and Technology of Computing Systems Group
Complutense University of Madrid

Computer Science School of UCM

ArTeCS hosted HPCA-10

Last February, from 14th to 18th, the Computer Science School (see picture) hosted the 10th International Symposium on High Performance Computer Architecture, HPCA-10, sponsored by IEEE Computer Society Technical Committee on Computer Architecture. HPCA has become one of the premier forums for presentation of research in all aspects of computer architecture, covering a wide range of topics, including processors, caches, memory and I/O issues as well as power management, prefetching and scheduling techniques.

ArTeCS crew at the Registration Desk

There were also six refereed workshops on:

- Embedded Parallel Architectures
- Network Processors
- System Area Networks
- Productivity and Performance in High-End Computing
- Computer Architecture Evaluation Using Commercial Workloads, and
- Interaction between Compilers and Computer Architecture.

Three tutorials studied some interesting topics in depth. The first one addressed Advanced Processor Architectures and Verification Challenges, presented by S. Kakkar from IBM Global Services, India. The second dealt with Power-Aware Design for High-Performance Processors, presented by J. Gonzalez, from Intel Barcelona Research Center, and K. Skadron, from the University of Virginia. The last one was on High-Performance Embedded Computing, by W. Wolf from Princeton University.

Francisco Tirado, from the Complutense University, and Emilio L. Zapata, from the University of Malaga, served as General Co-Chairs. Manuel Prieto and Luis Piñuel were responsible of local arrangements and, together with the rest of the ArTeCS team, worked very hard to have everything ready for the over two hundred participants. Almost half of them (49%) came from North-America, 35% from Spain, 11% from the rest of Europe and the remaining 7% from the rest of the World.

According with the high technical quality tradition of HPCA, the review process was very strict. José Duato, from Polytechnic University of Valencia served as Program Chair. Only 27 excellent papers out of 153 submissions were selected by the international program committee to be presented at the Symposium. There was industry collaboration in almost 40 % of the accepted papers, being Intel Research Labs., with 5 papers, the most interested company.

Yale Patt Keynote

The first two days of the Symposium, Saturday 14th and Sunday 15th, were devoted to the workshops and tutorials.

On Monday morning Yale Patt (see picture) opened the Symposium with the first keynote: Microarchitecture: Are we finally done?

Then came the regular sessions and a very hot panel: Bridging the research gap between academia and industry. The first day ended with a reception at the Town Hall (see picture) and a guided tour to the historical town.

Reception at the Town Hall

Tuesday began with the second keynote: Designing for the High End, by Steve Scott, from Cray. The day ended with a very interesting excursion to El Escorial (see picture) and the banquet.

On Wednesday, HPCA ended with two more keynotes: Kilo-Instructions In-Flight Processors, by Mateo Valero from Polytechnic University of Barcelona, and POWERS Architecture and Systems, by Balaram Sinharoy.

HPCA-11 will be held in San Francisco in 2005.

Visit to El Escorial

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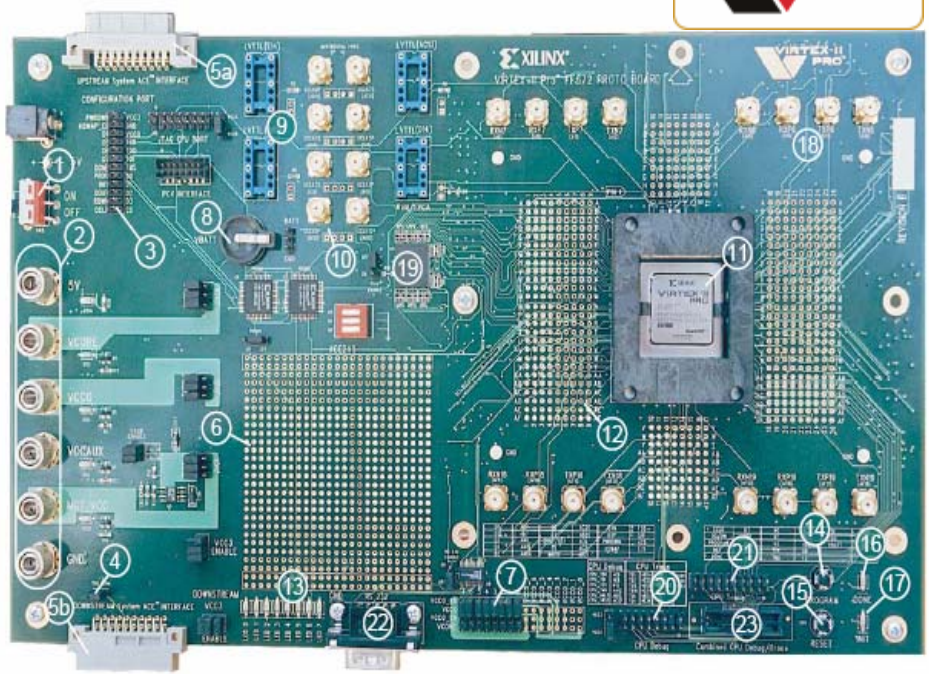
NoC emulation on FPGA

- Goal: Build a complete NoC emulation environment on FPGAs
- People involved:
  - From DACYA/UCM:
    - 2 PhD students: David Atienza, Javier B. Pérez
    - Assoc. Prof. José M. Mendías
    - Prof. Román Hermida
  - From other groups:
    - Nicolas Genko (LSI/EPFL)
    - Federico Angiolini (DEIS/Bologna)
- Additional students (since July – Sept. 2005):
  - 2 PhD students, 3 Master thesis students

ArTeCS

Hw/Sw Components & Tools Used

- Hardware: Virtex-II Pro Prototype Platform vp20 (2PPCs)
  (the same board in Bologna, donated by Xilinx)
- Software:
  - Xilinx EDK v6.3
  - Xilinx ISE v6.3
  - Mentor ModelSim v7.0
  - Synplicity Synplify Pro v7.3
  - Xilinx ChipScope v6.3



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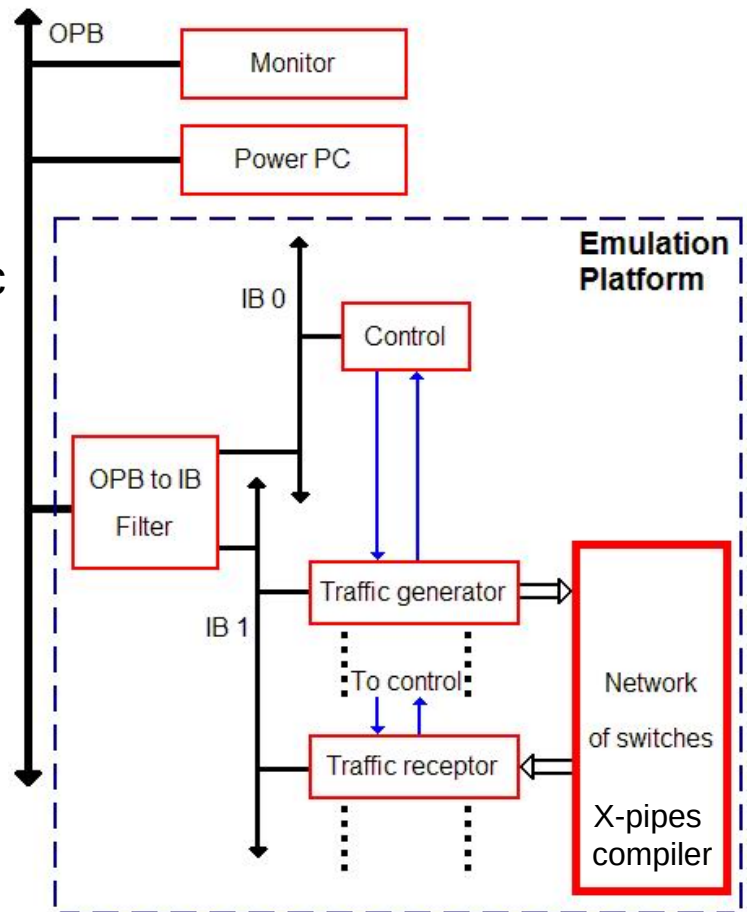
Current status NoC emulation framework (presented at DATE '05)

- 3 main parts:
  - Monitor (sends results to display)
  - Processor
  - Emulation platform
- Mixed HW/SW framework:
  - Sw running on PPC configures NoC traffic and statistics to be extracted.
  - A configurable topology of HW network of switches is emulated on an FPGA
- It allows:
  - Functional validation of networks of switches
  - Wide range of statistics about NoCs.
  - Enables emulation of real-life NoCs with millions of packets (50 MHz).
- New board: 6 switches use 32% of space



Planning (1/2)

- 1st Phase) Extension of TGs/TRs for using the new XPIPES protocol of the switches instead of the previous double-edge protocol. (3 weeks: Now – April 3rd)
  - VHDL version
  - Similar stochastic functionality as version from Stanford/EPFL (normal and bursts)
  - Documentation of how to use it
  - Additional stochastic models (work possibly done in Bologna)
- 2nd Phase) Extensions with OPB-OCP/PLB-OCP bridges for adding new cores. (2 weeks: April 3rd – April 17th).
  - Testing of OPB_OCP bridge to include some OPB cores (MicroBlaze, SRAM, …) (1 week: April 10th)
  - Creating the PLB_OCP bridge to put the PowerPC (1 week: April 17th)
- 3rd Phase) Extension of the Network Interfaces (With EPFL) (2 weeks: April 17th – May 1st)
  - Testing of NIs with some simple hand-made cores (1 week: April 24th)
  - Inclusion of some synthesizable OCP-compliant components from Bologna in the FPGA (S-RAM memory, FFT module, others to discuss...) (1 week: May 1st)

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Planning (2/2)

- 4th Phase) Porting of one application from the set used in Bologna in the MPARM emulator for NoC – ARM-based application

(2 weeks: May 1st – May 15th)

  - Multimedia or Network

- 5th Phase) Comparing NoC with bus-based interconnection topologies

(1 week: May 15th – May 22nd)

  - NoC topologies, buses of the FPGA, etc.

- 6th Phase) Adding first layers of the OSI protocol (in hw or sw)

(1 month: May 22nd – June 19th)

  - Mac layer or Network layer.

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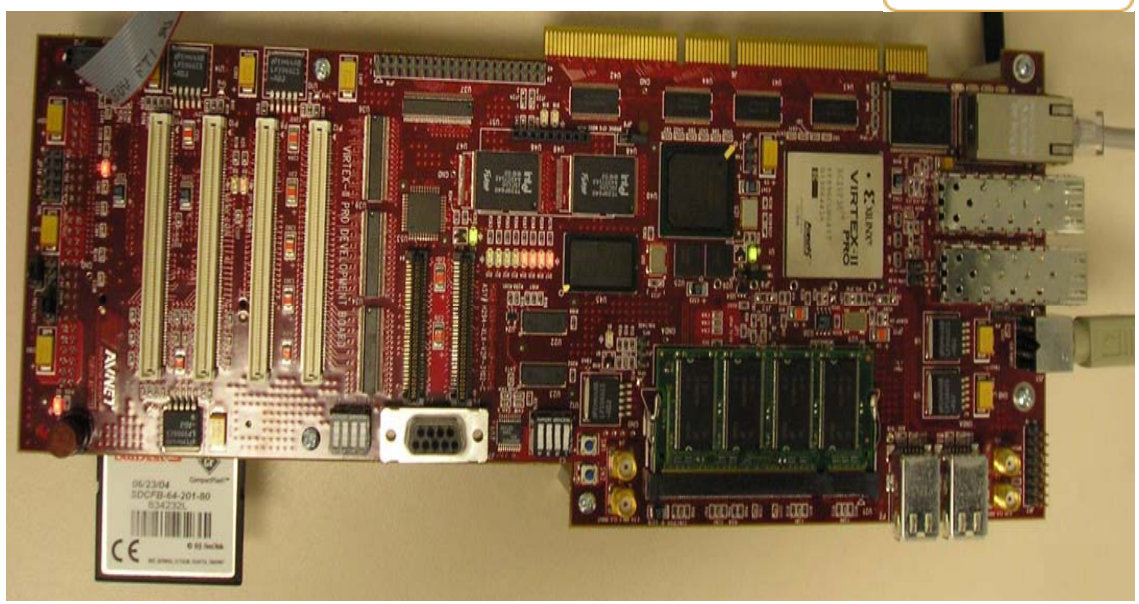
MpSoC emulation on FPGA

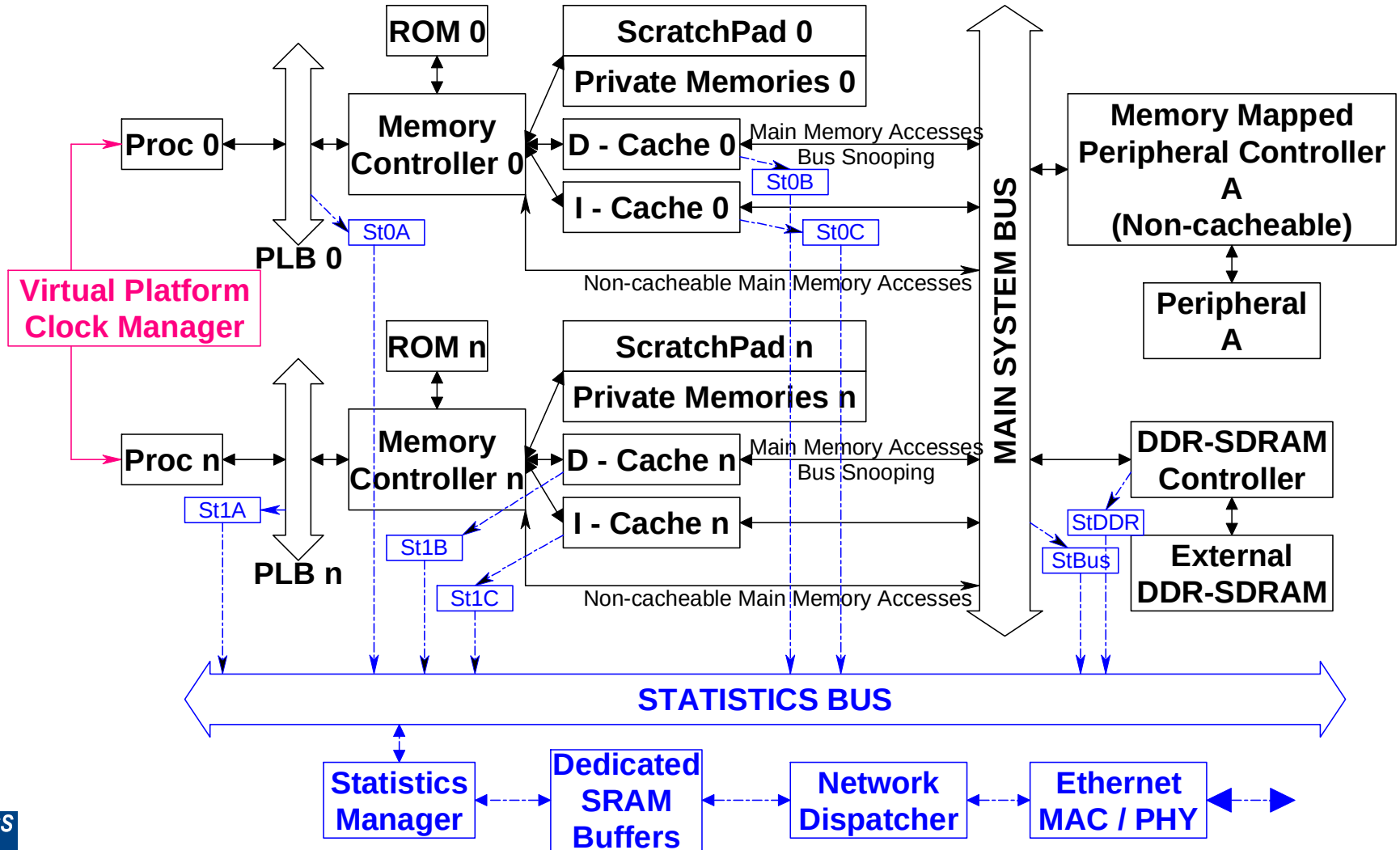
- Goal: MpSoC emulation and memory subsystem statistics extraction on FPGAs
- People involved:
  - From DACYA/UCM:
    - 3 Master Students: Esther Andrés, Pablo García, Javier García
    - 3 PhD students: David Atienza, Miguel Peón, Iván Magán
    - Assoc. Prof. José M. Mendías
    - Prof. Román Hermida
- Partners: DEIS/Bologna, DDT/IMEC, VLSILab/Xanthi
- Future additional collaborators (since July – Sept. 2005):
  - 1 PhD students, 3 Master thesis students

Hw/Sw Components & Tools Used

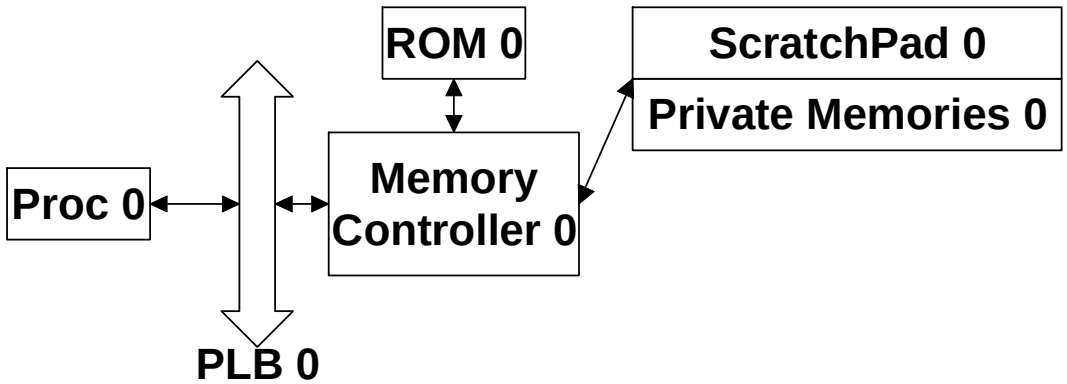
- Hardware: Virtex-II Pro XC2VP30-xFF896 manufactured by AVNET (2PPCs, Micron DDR SDRAM 128 MB expandable to 1GB, Micron Mobile SDRAM 32 MB, Cypress asynchronous SRAM 2 MB, Intel StrataFlash 16 MB, Compact FLASH card, Ethernet connection 10/100/1000 MBit/s Ethernet , PCI connector used with PCI-X core)
- Software:
  - Xilinx EDK v6.3
  - Xilinx ISE v6.3
  - Mentor ModelSim v7.0
  - Xilinx ChipScope v6.3
  - Xilinx CoreGen v6.3



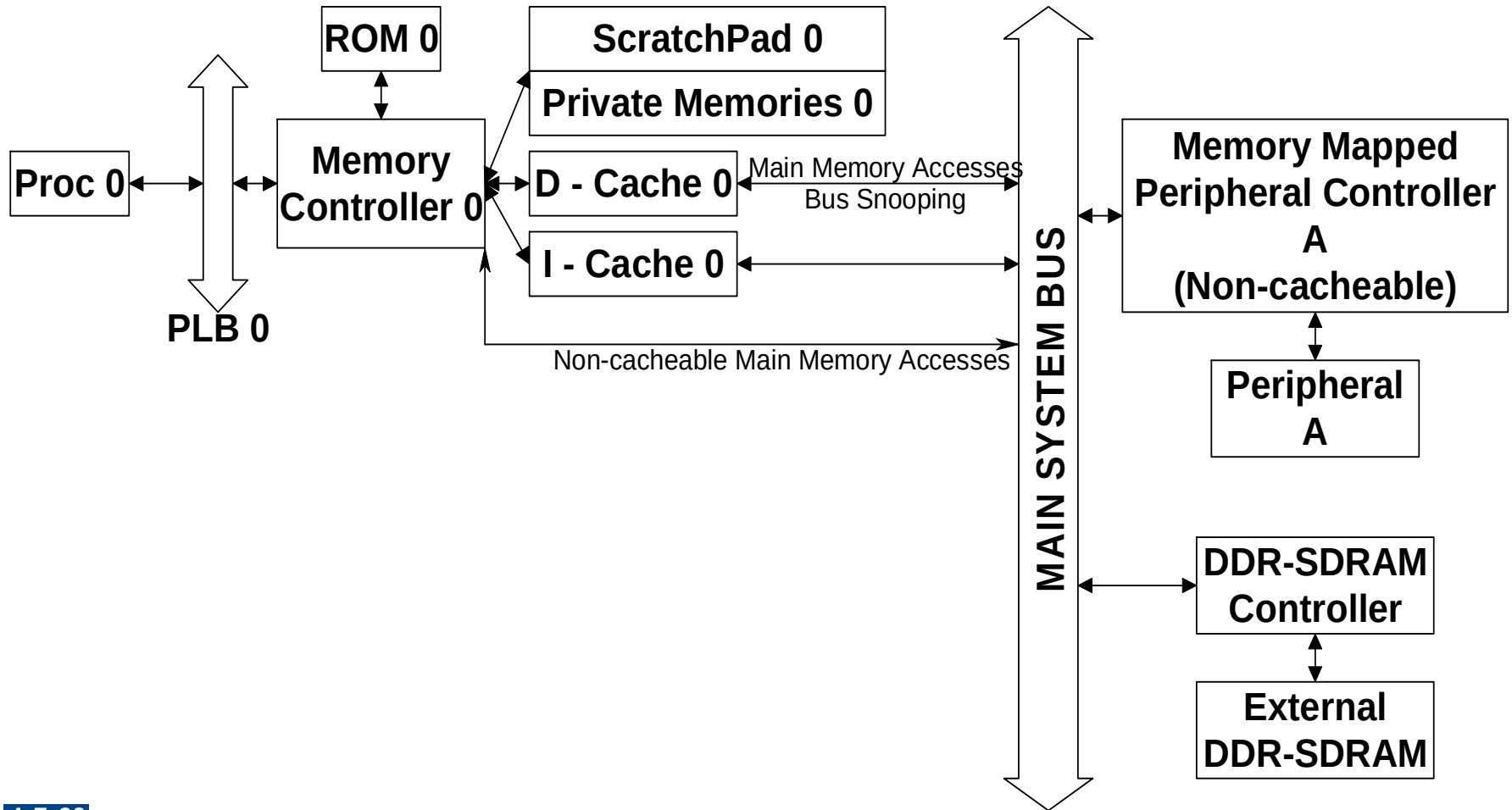
MPSoC HW Emulation Architecture



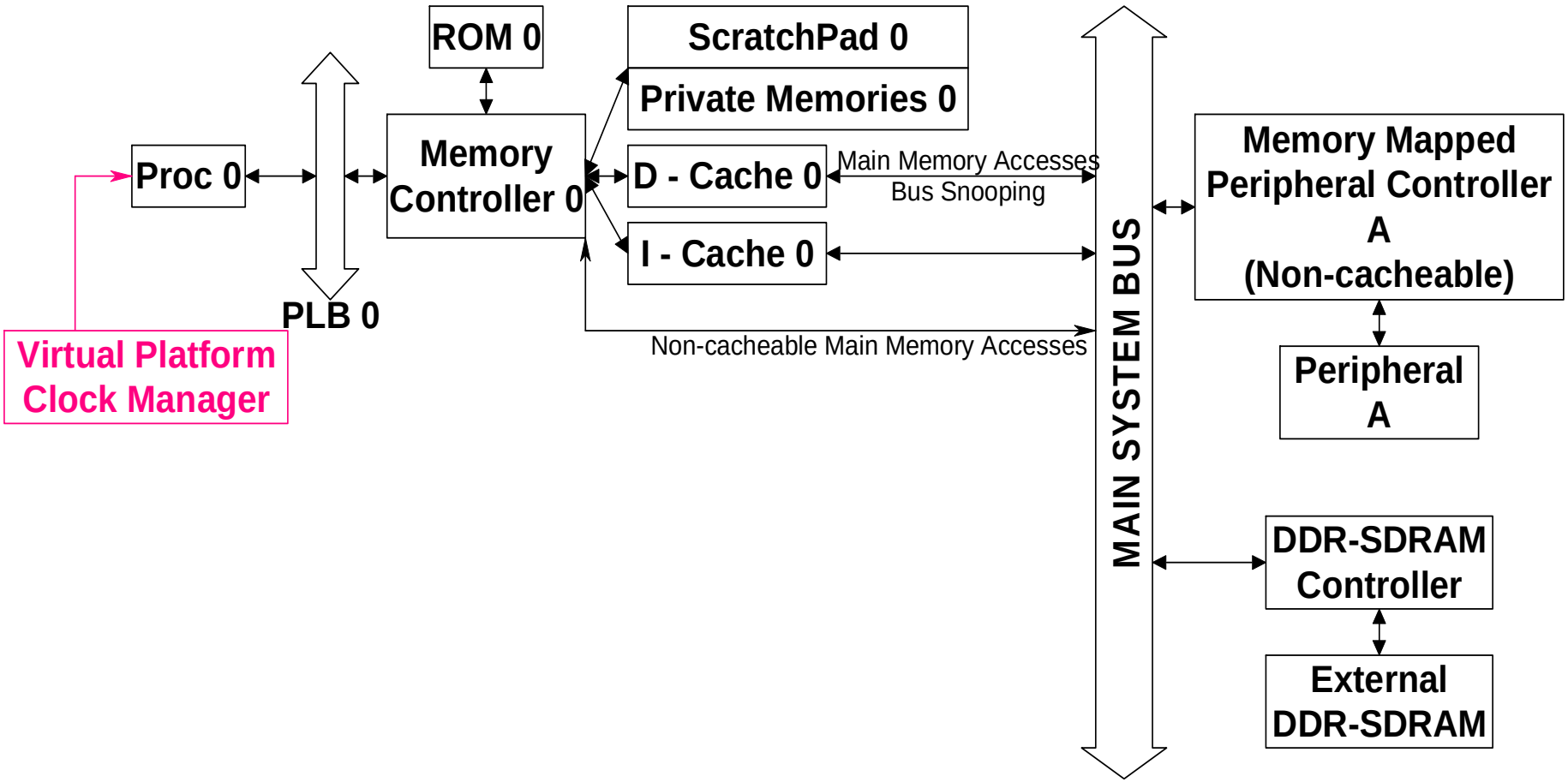
MPSoC HW Emulation Architecture (1/5)



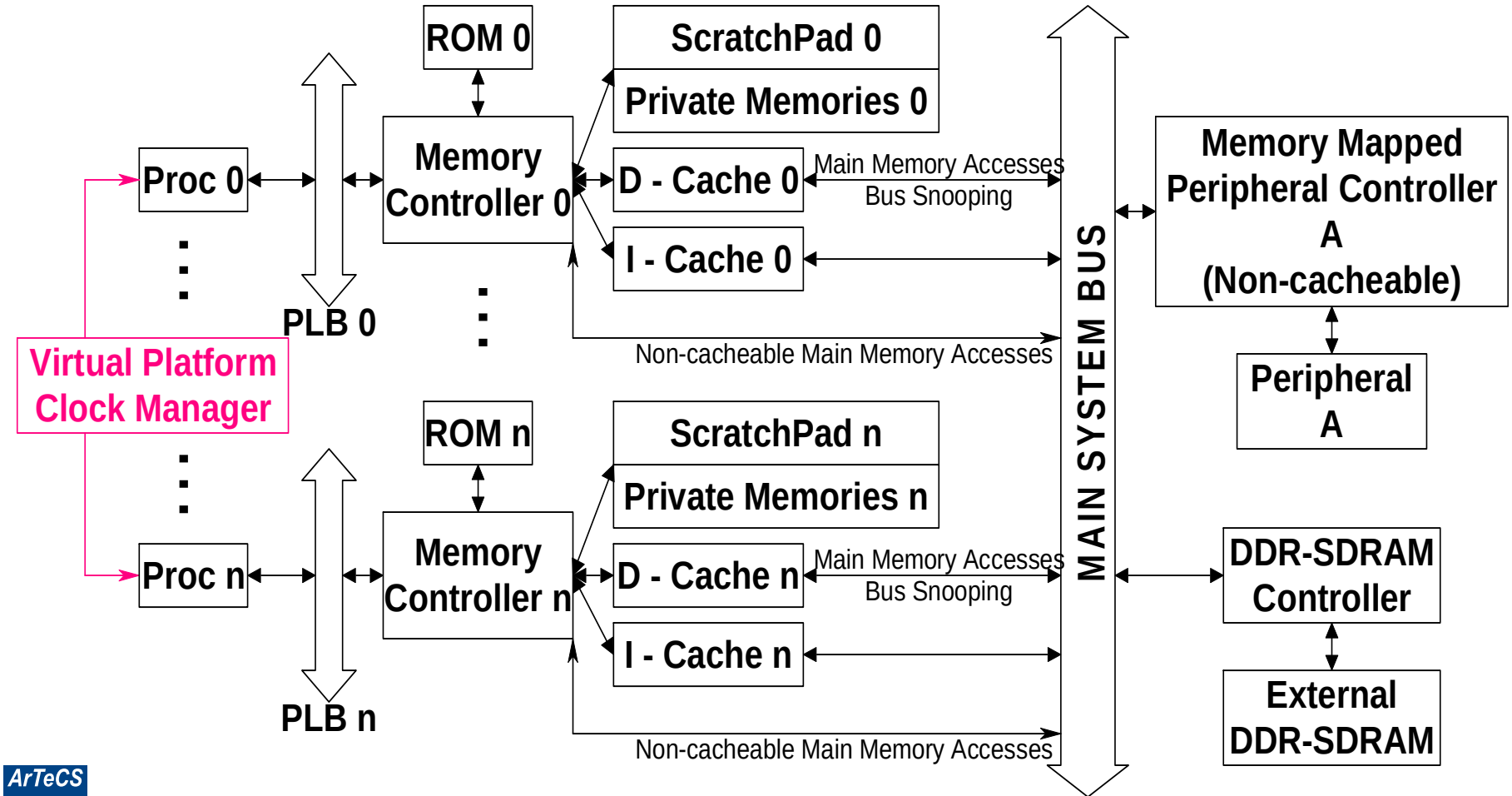
MPSoC HW Emulation Architecture (2/5)



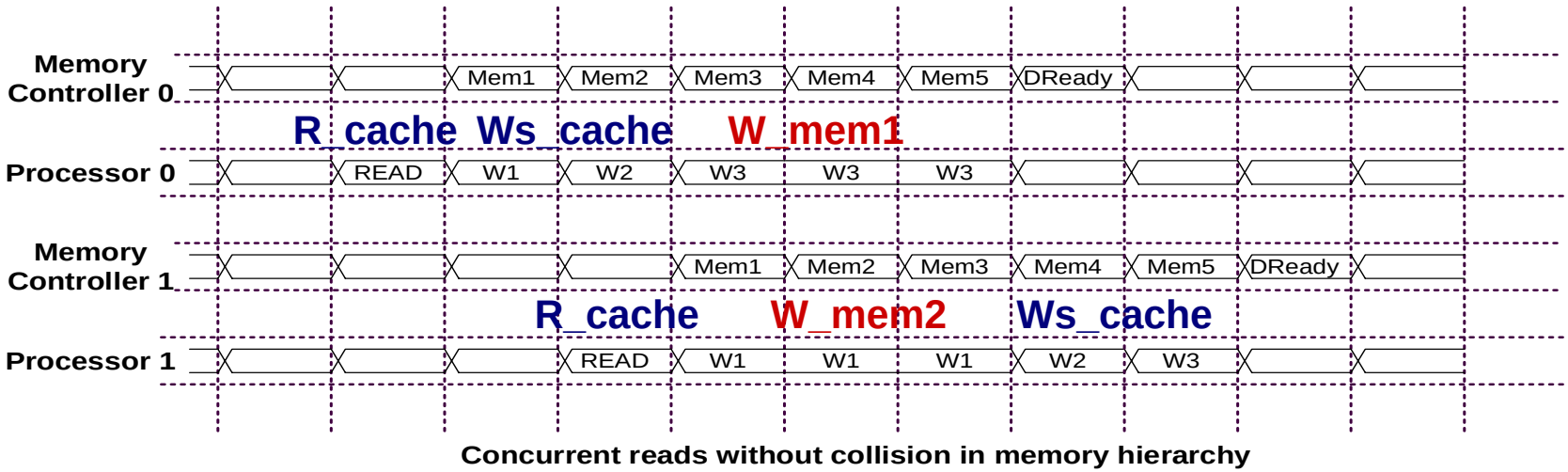
MPSoC HW Emulation Architecture (3/5)



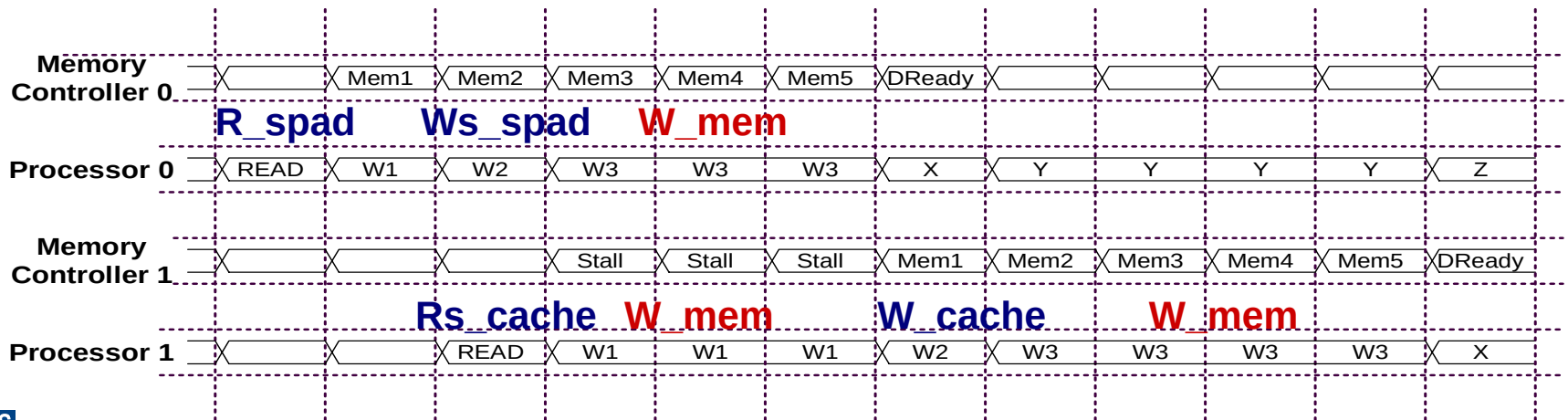
MPSoC HW Emulation Architecture (4/5)



Emulated Platform Clock Management



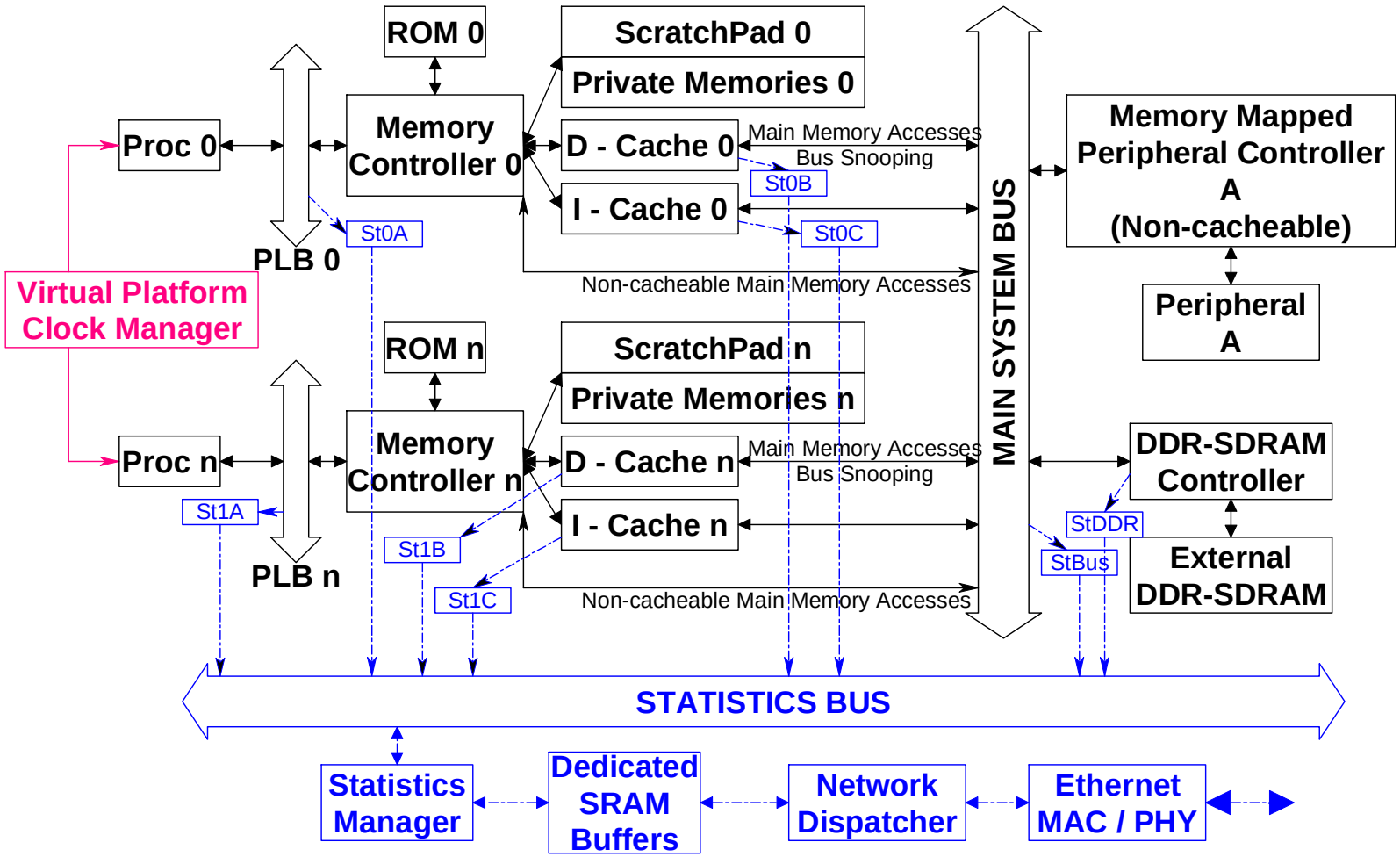
Concurrent reads without collision in memory hierarchy



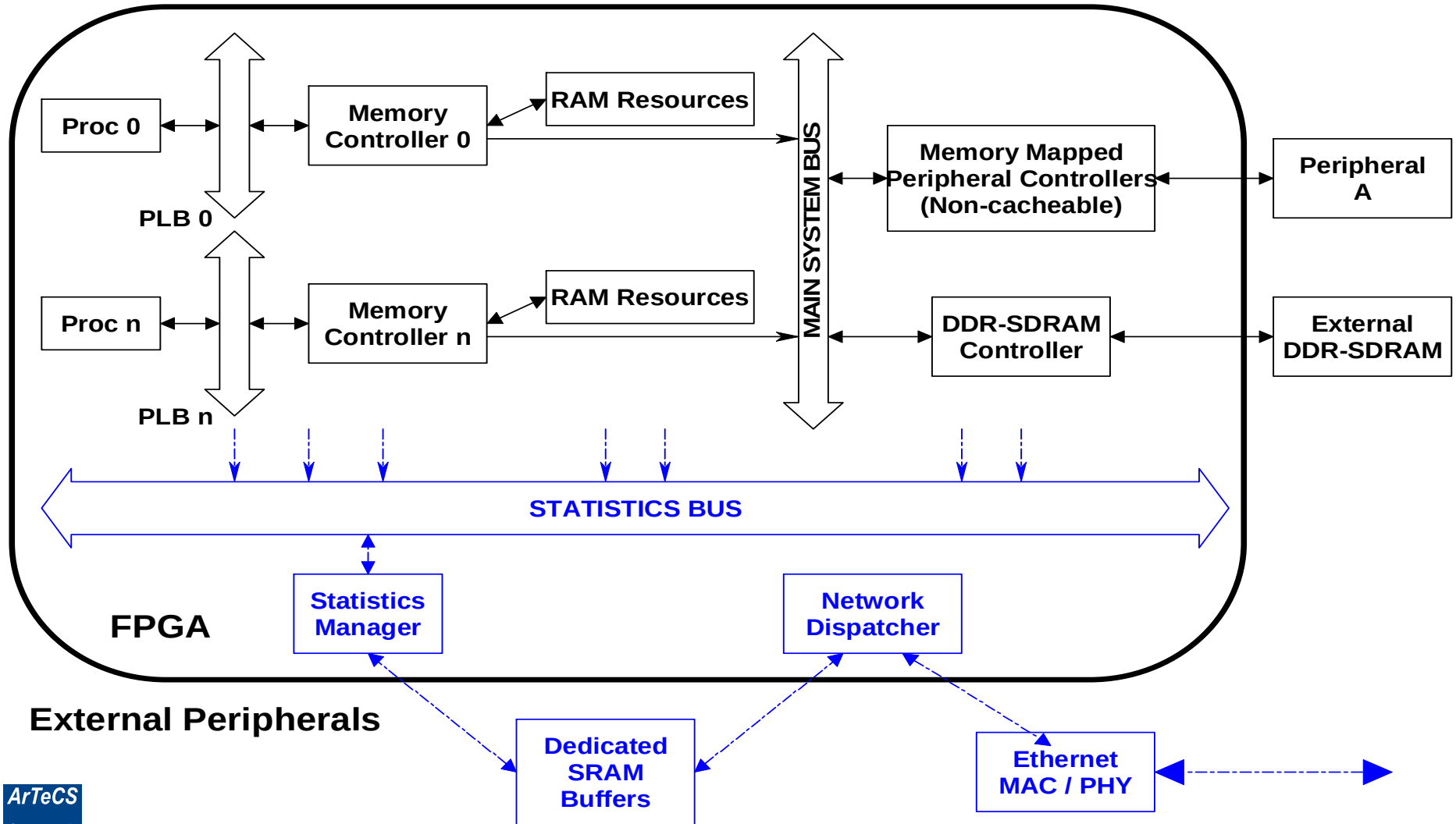
Concurrent reads wich collide in memory hierarchy

ArTeCS

MPSoC HW Emulation Architecture (5/5)

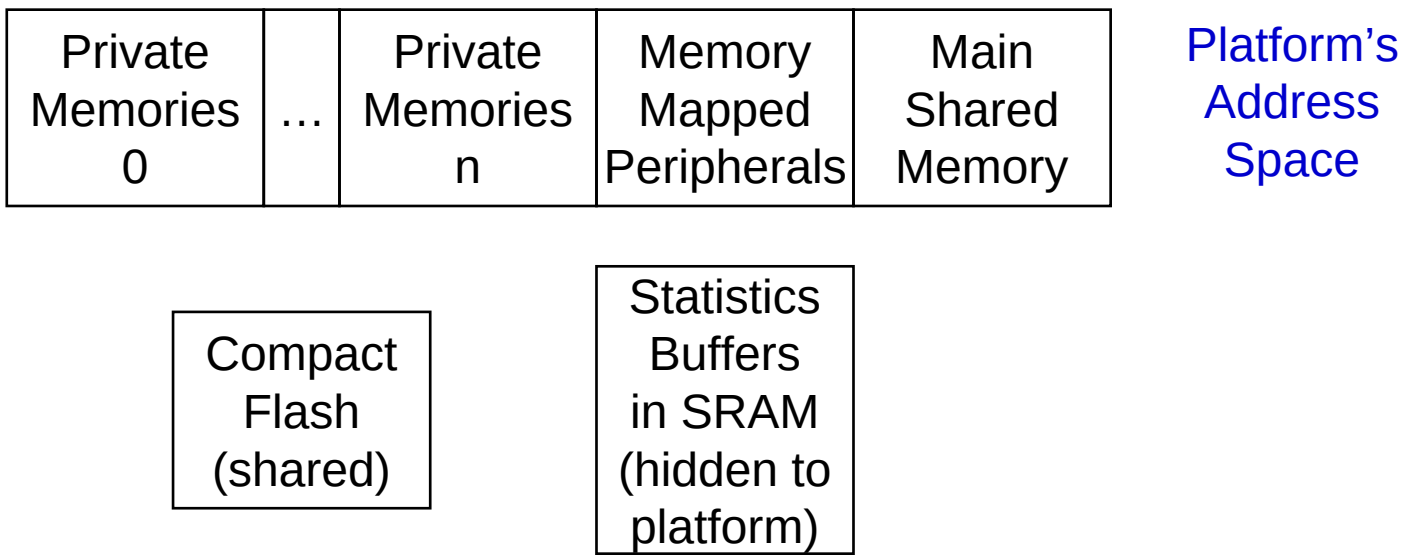


FPGA-Internal / External Resources



Platform Memory Map

- Emulated platform can access all levels of private or shared memories.
- It can also access Compact Flash resources.
- But cores cannot access SRAM buffers or Ethernet resources.



Main Features of Hw Architecture

- Clock signal for the emulated platform is generated by the emulation manager.
  - It allows the memory controllers to simulate any clock latencies that designers want to try.
  - It gives time to the statistics units to gather all the information and send it to the statistics manager through the statistics bus.
  - It allows to control emulation speed when network speed is not enough to dump the statistics buffer contents.
  - Emulated platform is stopped just when it is really needed to keep access times.
- The platform has emulation controllers for all resources available to the platform. Some of them are physically implemented with external devices, such as DDR-SDRAMs and serial port connections.

Main Features of Sw Architecture

- ROM boot loader runs into each PPC and loads Linux image from Compact Flash card into DDR-SDRAM through virtual platform resources.
- ROM boot loader jumps to the Linux kernel entry-point.
- Linux starts execution and initializes resources.
- Applications under development can be put inside the OS image or downloaded over serial connection.
- Application SW can call library functions to start / stop statistics gathering.

Planning (1/2)

- 1st Phase) Addition of DDR memory to the memory hierarchy

  (Three weeks: Now – April 3rd)
  - Testing of OPB_DDR (1 week: March 20th)
  - Development of PLB_DDR (1 week: March 27th)
  - Development of buffer for mpSoC to avoid continuous page preloading (3 days: March 30th)
  - Testing of complete memory hierarchy (4 days: April 3rd)
- 2nd Phase) Statistics extraction through Ethernet connection

  (One month approx.: April 3rd – May 8th)
  - Sniffers in VHDL version (1 week: April 10th)
  - Centralized collector module of statistics (2 weeks: April 24th)
  - Testing of Ethernet statistics extraction system (2 weeks: May 8th)

Planning (2/2)

- 3rd Phase) Porting of ucLinux OS from AVNet.

  (Two months: May 8th – July 3rd)
  - Development of boot mechanisms for Linux from CompactFlash card

  (1 week: May 15th)
  - Testing current version of ucLinux on the FPGA

  (1 week: May 22nd)
  - Development of new drivers for the additional components of FPGA

  (2 weeks: June 5th)
  - Testing new porting of ucLinux

  (2 week: June 19th)
  - Documentation of how to use/extend it (with DEIS/Bologna, DDT/IMEC)

  (2 weeks: July 3rd)

- Next year) Addition of other cores (URLAUB/ARM4 collaboration EPFL)
  - VHDL code available
  - Test chips implemented on real platform at LAP/EPFL

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Asynchronous System Team/ArTeCS

- People involved:Three doctors and three PhD. students
- Three lines of research
  - Asynchronous protocols between cores
  - Globally Asynchronous–Locally Synchronous multi-clock domain systems (GALS) with Simultaneous Multi-Threading (SMT)
  - Application of asynchronous techniques to low-power
- Background:
  - FPGA: Virtex XC2V, SPARTAN XC2S, Multi-FPGA systems (Ph.D. thesis on this subject)
  - HDL: Verilog, VHDL, SystemC, e-language
  - Tools: Synopsys (design compiler, Primetime, Tetramax, Formality, …), Verilog-XL, Verilint, Verisity Specman, Modelsim, Xilinx ISE 6.0, SimpleScalar & Wattch
  - Industrial environment experience: Agere Systems, TSMC 0.13 µm

ArTeCS

Asynchronous Protocols Between Cores

- Goal: establish new methods to accelerate the computations
- Communication protocol definitions
  - No clocks, event-driven. Avoids metastable behaviors in the communication between temporization domains.
  - Validated using Petri Nets (tested on Spartan FPGAs).
- Computation Completion
  - Data Classification based on Data Latency (DCDL)
    - Define classes of input vectors based on their latencies. Associate a different delay with each class.
    - Combine these two ideas (Protocol+DCDL) in the design of a GALS DLX-like processor
- Current status
  - First GALS DLX-like simulator done
  - Evaluating more aggressive DCDL techniques
- Next milestone
  - New ideas: Monitoring combinational logic activity to speedup asynchronous protocols

GALS with SMT

- Goal: evaluate the GALS paradigm on SMT processors.
- Merge both paradigms
  - Globally Asynchronous–Locally Synchronous Multi-Clock Domain systems (GALS-MCD)
  - Simultaneous Multi-threading processors (SMT)
- Joint effort of DACYA/UCM and University of Rochester
- Development platform
  - Asynchronous SimpleScalar
- Current status
  - Customizing the simulator
- Next milestones
  - Simulator v1.0. End of July
  - Architectural exploration of the processor
    - Performance and power-consumption evaluation
    - Bottlenecks identification

Low-Power Techniques in GALS

- Goal: reduce power-consumption on Asynchronous Processors
- Evaluation Platform
  - Asynch. SimpleScalar from University of Rochester & Wattch
- Current status
  - Customizing SimpleScalar to properly model power-consumption of all asynch. FU's
  - Applying pseudo-asynchronous techniques to integer FUs
    - Classifying input data into classes and using customized FUs
    - Coding new scheduling policies according to FU features
- Next milestones
  - Performance and power-consumption evaluation
  - Extend this method wherever it is possible

Conclusions

- New version of NoC emulation platform coming soon
  - VHDL version
  - New protocol of Xpipes used in TGs/TRs, PPC running applications
  - Additional layers (in hw/sw) added by Summer
- Possible to emulate MpSoC systems in Virtex-II Pro boards
  - Now using Xilinx hw components (PPC, PLB and OPB bus…) and sw components (ucLinux porting from AVNet)
  - Currently possible to compile real applications with some restrictions (e.g. no OS, no VGA output)
- Emulation extensions with asynchronous techniques
  - Collaboration with asynchronous systems team at DACYA/UCM
  - Including GALs and asynchronous low-power techniques